



INFORMATION DISCLOSURE STATEMENT

Applicant : Brabant et al.
App. No : 10/800,390
Filed : 12 March 2004
For : EPITAXIAL SEMICONDUCTOR DEPOSITION
METHODS AND STRUCTURES
Examiner : David Vu
Art Unit : 2818

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a PTO/SB/08 Equivalent listing 41 references to be considered by the Examiner. Also enclosed are 30 foreign patent references and/or non-patent literature as listed on the Information Disclosure Statement.

This Information Disclosure Statement is being filed before the mailing date of a final action and before the mailing of a Notice of Allowance. This Statement is accompanied by the fees set forth in 37 C.F.R. § 1.17(p). The Commissioner is hereby authorized to charge any additional fees which may be required or to credit any overpayment to Account No. 11-1410.

Respectfully submitted,
KNOBBE, MARTENS, OLSON & BEAR, LLP

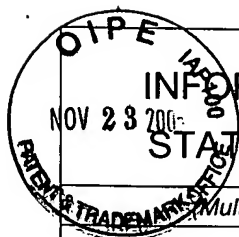
Dated: 21 nov 05

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Multiple sheets used when necessary)

SHEET 1 OF 4

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First Named Inventor	Paul D. Brabant
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Examiner	David Vu
Attorney Docket No.	ASMEX.448A

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	5,221,556	06/22/93	Hawkins et al.	
	2	5,879,970	03/09/99	Shiota et al.	
	3	6,093,252	07/25/00	Wengert et al.	
	4	6,319,782	11/20/01	Nakabayashi	
	5	6,373,112	04/16/02	Murthy et al.	
	6	6,537,370	03/25/03	Hernandez et al.	
	7	6,592,942	07/15/03	Van Wijck	
	8	2002/0173130	11/21/02	Pomerede et al.	
	9	2003/0190791	10/09/03	Fischetti, et al.	
	10	2003/0235931	12/25/03	Wada et al.	
	11	2004/0219735	11/04/04	Brabant et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	12	WO 01/41544	06/14/01	PCT		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
	13	BAUER et al., "Relaxed SiGe buffers with thicknesses below 0.1 μm ", <i>Thin Solid Films</i> 369:152-156 (2000).	
	14	BAUER et al., "High Ge content photodetectors on thin SiGe buffers", <i>Materials Science and Engineering B89</i> :77-83 (2002).	
	15	BENSAHEL et al., "Single-wafer processing of in-situ doped polycrystalline Si and Si _{1-x} Ge _x ", <i>Solid State Technology</i> , pages S5-S10 (March 1998).	

Examiner Signature	Date Considered
<p>*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	

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	16	CHUI et al., "Ultrathin high-k gate dielectric technology for germanium MOS applications", <i>IEEE 60th Annual Device Research Conference (DRC) Digest</i> , paper VII.B2, pages 191-192 (2002).	
	17	COLACE et al., "Ge/Si(001) photodetector for near infrared light", <i>Solid State Phenomena</i> 54:55-58 (1997).	
	18	COLACE et al., "Metal-semiconductor-metal near-infrared light detector based on epitaxial Ge/Si", <i>Applied Physics Letters</i> 72:3175-3177 (1998).	
	19	COLACE et al., "Metal-Ge-Si diodes for near-infrared light detection", <i>Journal of Vacuum Science and Technology B</i> 17:465 (1999).	
	20	CURRIE et al., "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing", <i>Applied Physics Letters</i> 72:1718-1720 (1998).	
	21	FISCHETTI et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys", <i>Journal of Applied Physics</i> 80:2234-2252 (1996).	
	22	GIOVANE et al., "Correlation between leakage current density and threading dislocation density in SiGe p-i-n diodes grown on relaxed graded buffer layers", <i>Applied Physics Letters</i> 78:541-543 (2001).	
	23	HARTMANN et al., "Reduced pressure-chemical vapor deposition of Ge thick layers on Si(001) for 1.3-1.55-μm photodetection", <i>Journal of Applied Physics</i> 95:5905-5913 (2004).	
	24	JACKSON et al., "Gate-Self-Aligned p-Channel Germanium MISFET's", <i>IEEE Electron Device Letters</i> 12:605-607 (1991).	
	25	KASPER, "Prospects of SiGe Heterodevices", <i>Journal of Crystal Growth</i> 150:921-925 (1995).	
	26	KASPER et al., "New virtual substrate concept for vertical MOS transistors", <i>Thin Solid Films</i> 336:319-322 (1998).	

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	27	LEE et al., "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on Si _{1-x} Ge _x /Si virtual substrates", <i>Applied Physics Letters</i> 79:3344-3346 (2001).	
	28	LEE et al., "Strained Si/strained Ge dual-channel heterostructures on Relaxed Si _{0.5} Ge _{0.5} for symmetric mobility p-type and n-type metal-oxide-semiconductor field-effect transistors", <i>Applied Physics Letters</i> 83:4202-4204 (2003).	
	29	LEE et al., "Electron mobility characteristics of n-channel metal-oxide-semiconductor field-effect transistors fabricated on Ge-rich single- and dual-channel SiGe heterostructures", <i>Journal of Applied Physics</i> 95:1550-1555 (2004).	
	30	LETERTRE et al., "Germanium-on-insulator (GeOI) structure realized by the Smart Cut™ technology", <i>MRS Proceedings</i> , vol. 809 (2004).	
	31	LUAN et al., "High-quality Ge epilayers on Si with low threading-dislocation densities", <i>Applied Physics Letters</i> 75:2909-2911 (1999).	
	32	LYUTOVICH et al., "Interaction between point defects and dislocations in SiGe", <i>Solid State Phenomena</i> 69-70:179-184 (1999).	
	33	LYUTOVICH et al., "Relaxed SiGe buffer layer growth with point defect injection", <i>Materials Science and Engineering B</i> 71:14-19 (2000).	
	34	LYUTOVICH et al., "Thin SiGe buffers with high Ge content for n-MOSFETs", <i>Materials Science and Engineering B</i> 89:341-345 (2002).	
	35	NI et al., "X-ray reciprocal space mapping studies of strain relaxation in thin SiGe layers (≤100 nm) using a low temperature growth step", <i>Journal of Crystal Growth</i> 227-228:756-760 (2001).	
	36	REINKING et al., "Ge p-MOSFETs compatible with Si CMOS-technology", <i>Proceedings of the 29th ESSDERC</i> 99:300-303 (1999).	
	37	SAMAVEDAM et al., "High-quality germanium photodiodes integrated on silicon substrates using optimized relaxed graded buffers", <i>Applied Physics Letters</i> 73:2125-2127 (1998).	

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	38	SCHÖLLHORN et al., "Coalescence of germanium islands on silicon", <i>Thin Solid Films</i> 336:109-111 (1998).	
	39	SHANG et al., "Electrical characterization of germanium <i>p</i> -channel MOSFETs", <i>IEEE Electron Device Letters</i> 24:242-244 (2003).	
	40	THOMAS et al., "Structural characterization of thick, high-quality epitaxial Ge on Si substrates grown by low-energy plasma-enhanced chemical vapor deposition", <i>Journal of Electronic Materials</i> 32:976-980 (2003).	
	41	"Physics of Thin Films", printed from http://www.uccs.edu/~tchrste/courses/PHYS549/549lectures/film2.html (22 Feb 00).	

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